

WHAT IS CLAIMED IS:

1. An image processing circuit processing raw image data picked up with an image pickup device, comprising:

5 compression means compressing digital image data obtained by A/D converting said raw image data;

 a buffer part temporarily storing compressed data transferred from said compression means;

 expansion means reading said compressed data from said buffer part and
10 expanding the same; and

 an image processing part executing image processing on expanded data transferred from said expansion means.

2. The image processing circuit according to claim 1, wherein said image
15 pickup device is driven by an interlacing system reading an odd field consisting of only odd lines and an even field consisting of only even lines forming a frame at temporally different timings,

 said buffer part stores said compressed data of a first field formed by either said odd field or said even field, and

20 said image processing part reads said first field stored in said buffer part in synchronization with entry of a second field formed by remaining said field and executes real-time image processing on said first and second fields.

3. The image processing circuit according to claim 1 or 2, wherein
25 data transfer between said compression means and said buffer part, and data

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Related Pending Application
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transfer between said expansion means and said buffer part are controlled by a direct memory access system.

4. The image processing circuit according to claim 1, further comprising
5 division means dividing said digital image data into a plurality of blocks and outputting the same to said compression means, wherein

said compression means and said expansion means execute compression and expansion in units of said blocks.

10 5. The image processing circuit according to claim 4, further comprising means detecting a block including previously specified defective pixel data among said expanded data expanded by said expansion means and outputting a block obtained by correcting said defective pixel data to said compression means.

15 6. The image processing circuit according to claim 4, further comprising defect inspection/correction means performing a defect inspection before outputting said expanded data expanded by said expansion means to said image processing part for replacing a block having detected defective pixel data with a normal block and outputting the same to said compression means.

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7. The image processing circuit according to any of claims 4 to 6, wherein
said division means divides said digital image data into a plurality of blocks in units of lines.

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8. The image processing circuit according to claim 1 or 2, further comprising

difference calculation means calculating the difference between pixel values of said digital image data and outputting said difference to said compression means before compressing said digital image data in said compression means.

5 9. The image processing circuit according to claim 8, wherein
said difference calculation means calculates the difference between the values
of pixels adjacent to each other along the time base.

10 10. The image processing circuit according to claim 8, wherein
said difference calculation means calculates the difference between the values
of alternate pixels along the time base.

15 11. The image processing circuit according to claim 8, wherein
said difference calculation means calculates the difference between the values
of vertically adjacent two pixels of two lines of said digital image data.

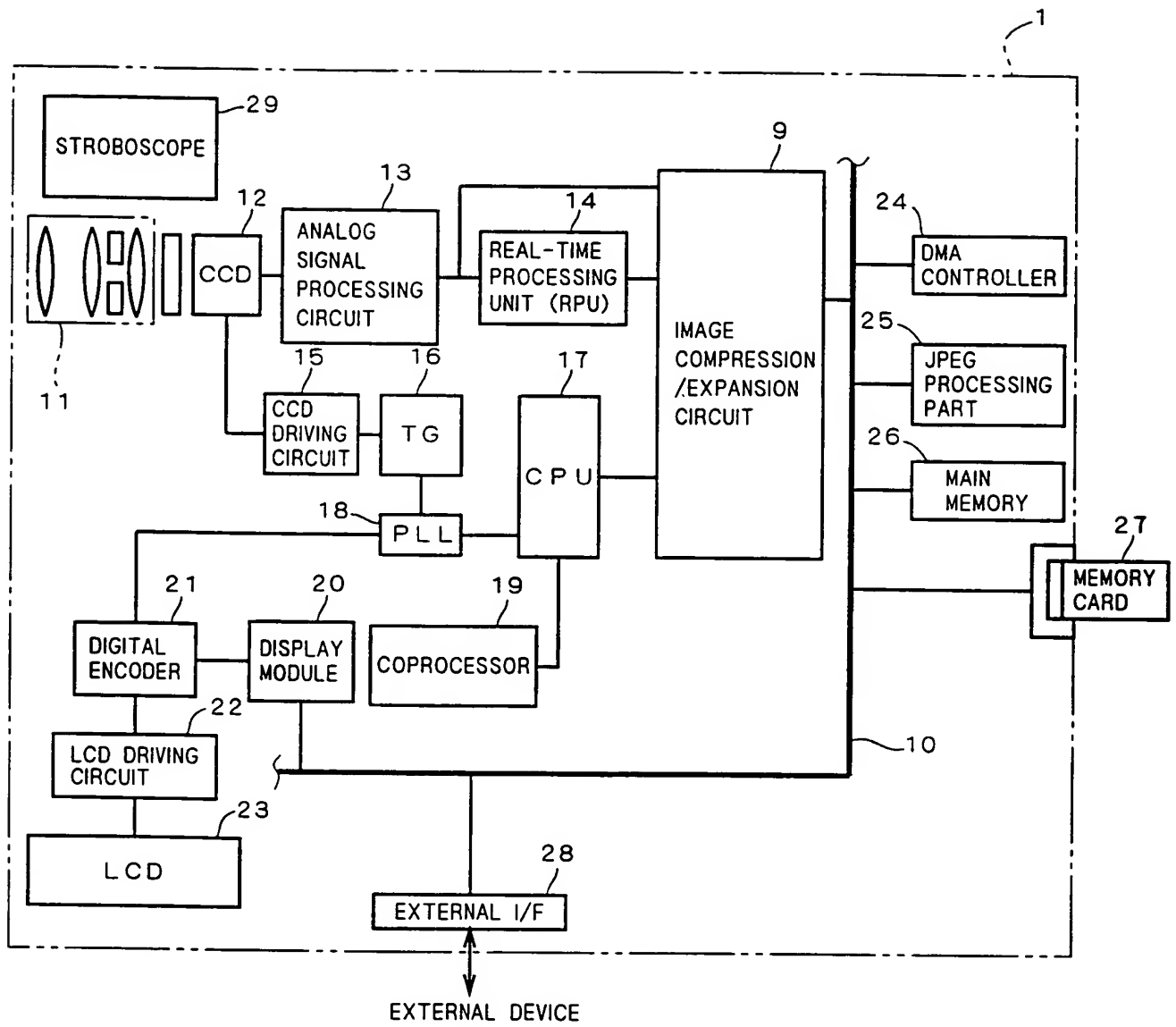
20 12. The image processing circuit according to claim 8, wherein
said difference calculation means calculates the difference between the values
of vertically adjacent two pixels of alternate lines of said digital image data.

 13. The image processing circuit according to claim 8, wherein
said difference calculation means according to either claim 11 or claim 12 is
selected in response to the driving system for said image pickup device.

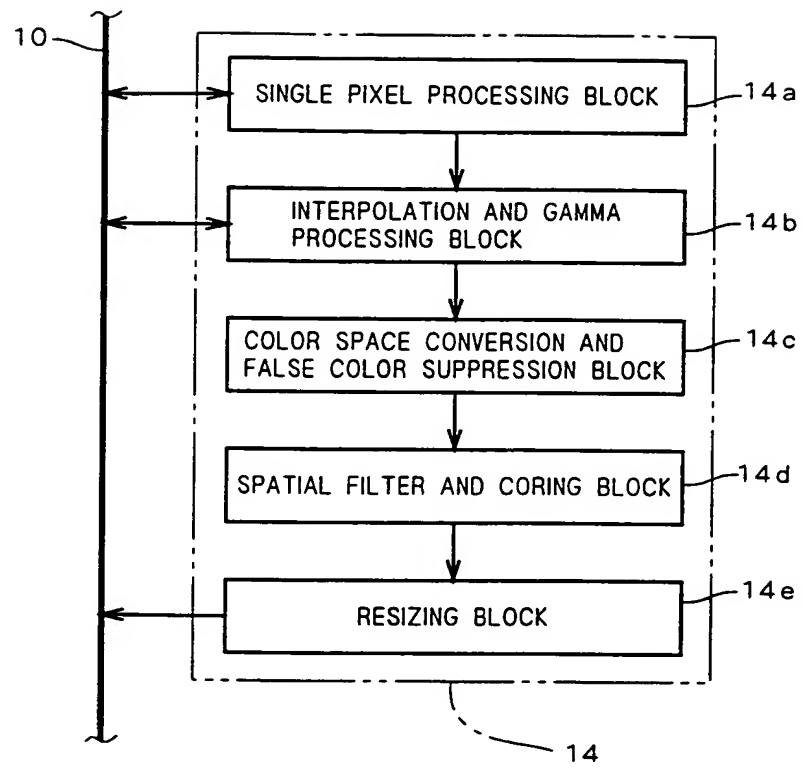
ABSTRACT OF THE DISCLOSURE

CCD data is compressed by compression means and stored in a raw image data buffer (step 10). Then, the compressed data is expanded by expansion means, so that pixel data thereof is sequentially output to an RPU (step 11). The RPU executes
5 real-time image processing on the pixel data, so that the processed data is stored in a processed data buffer in units of frames. Then, a CPU reads an image from the processed data buffer at a proper timing and performs software processing such as high-efficiency coding through a temporary storage data buffer, for storing and preserving the processed data in a storage medium (step 12). Thus provided is an image
10 processing circuit capable of reducing the scale of buffer areas in a memory for remarkably reducing the cost for the memory as well as power consumption.

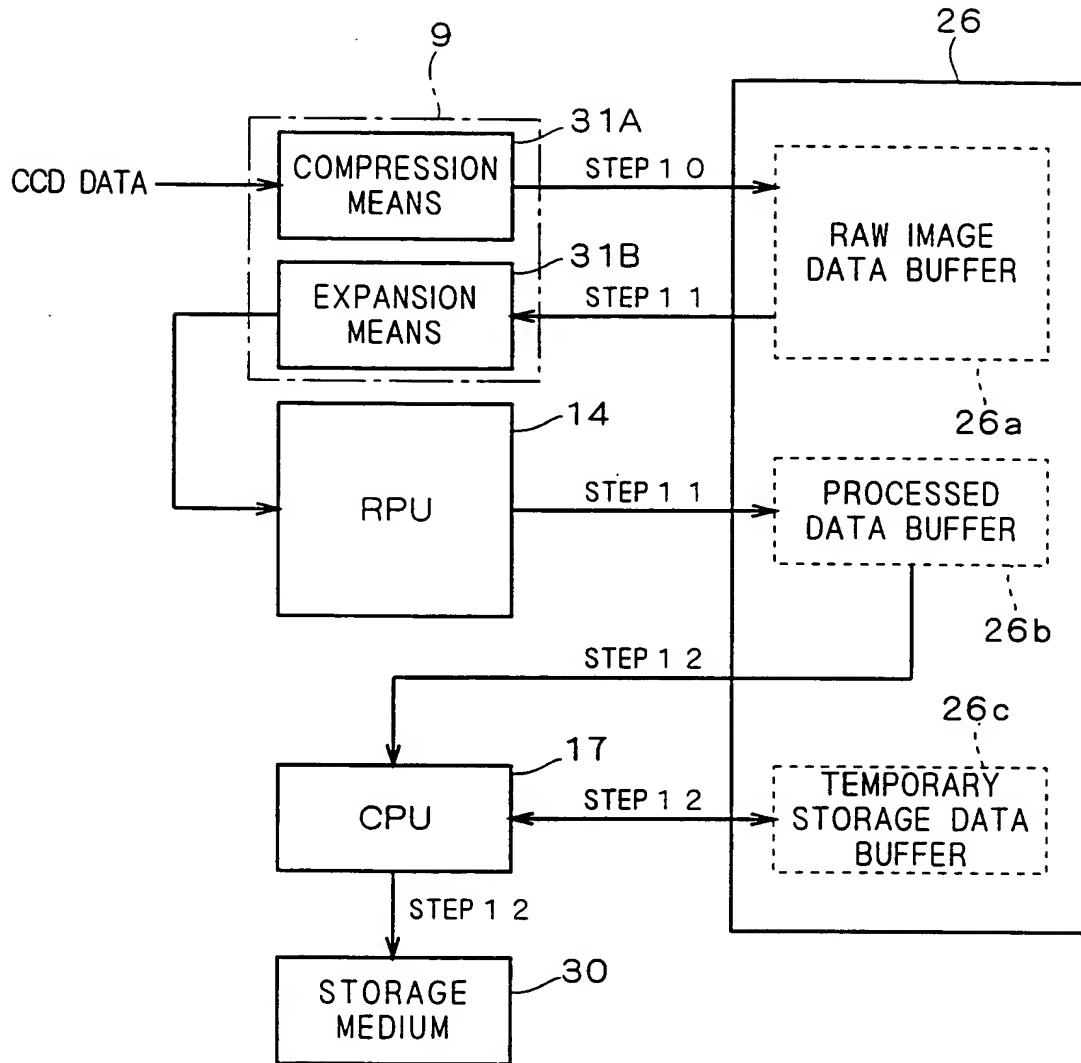
F I G . 1



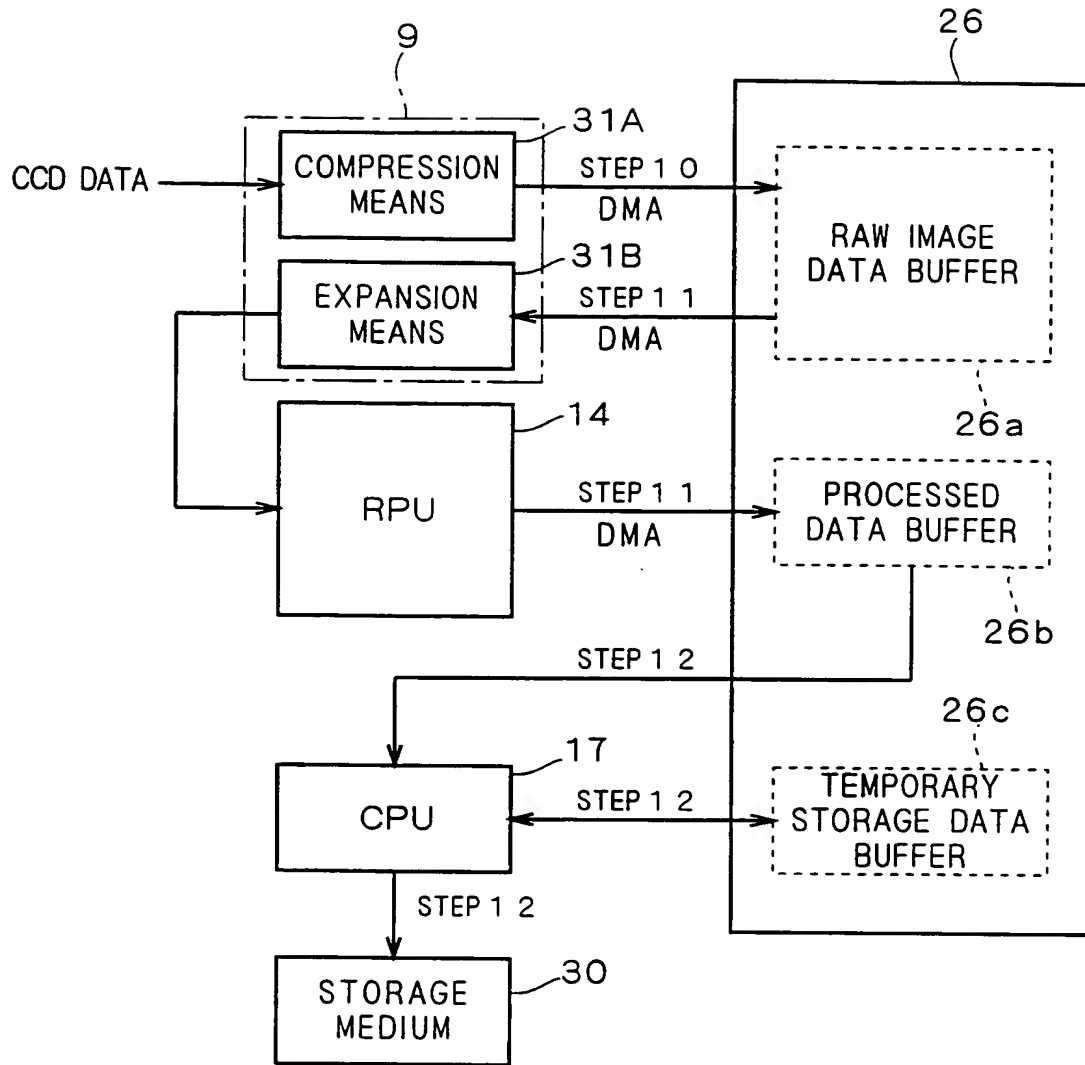
F I G . 2



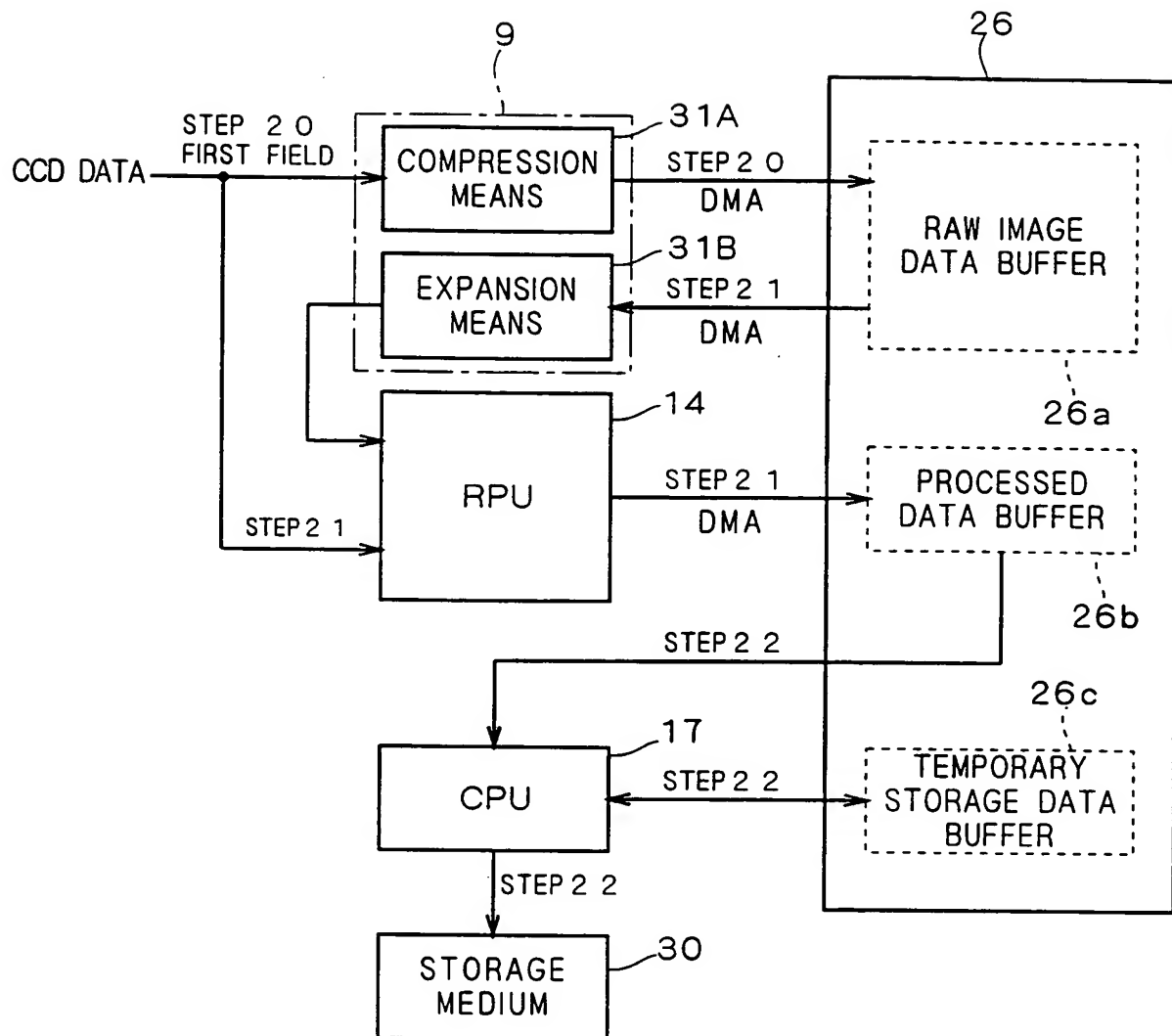
F I G . 3



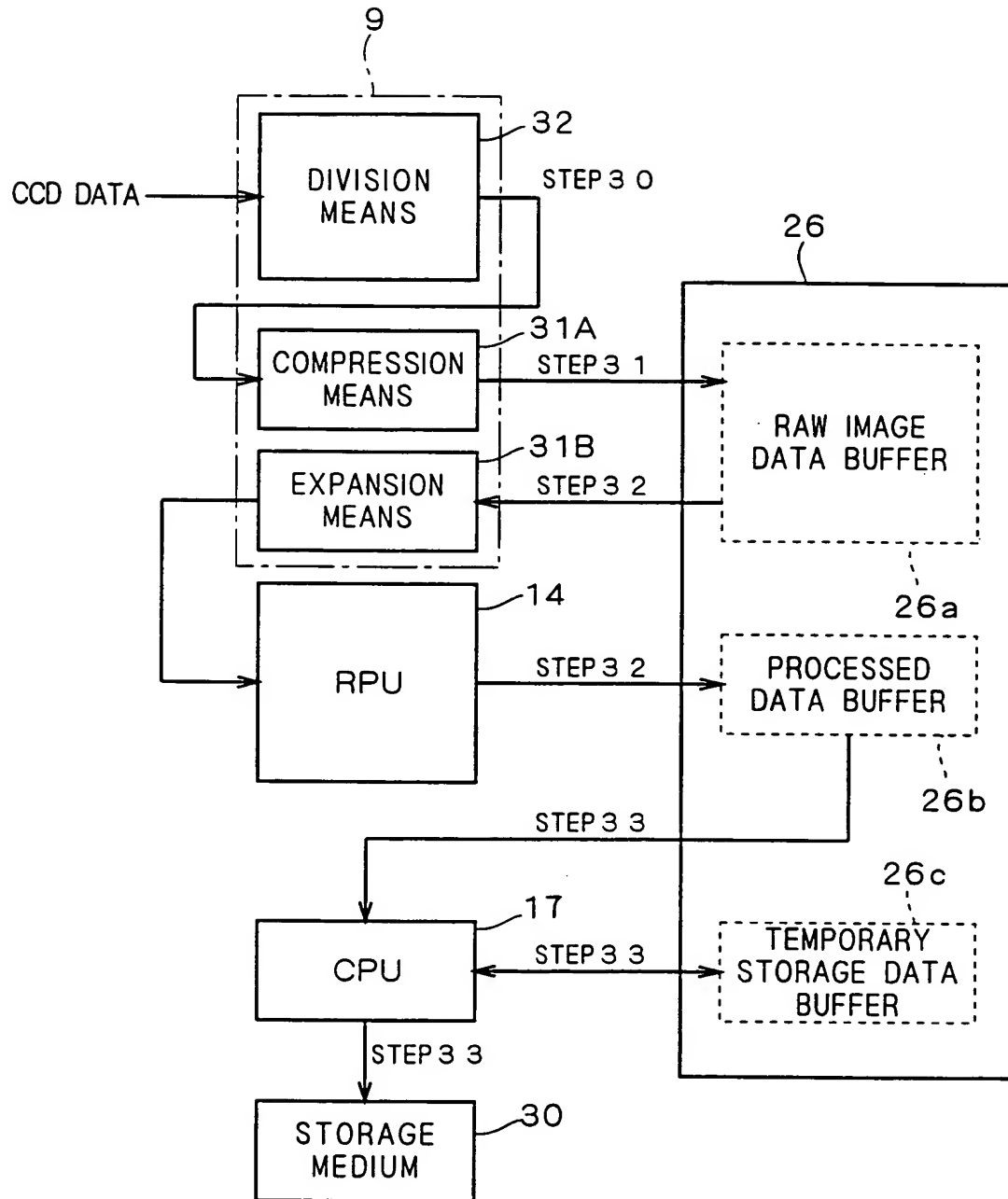
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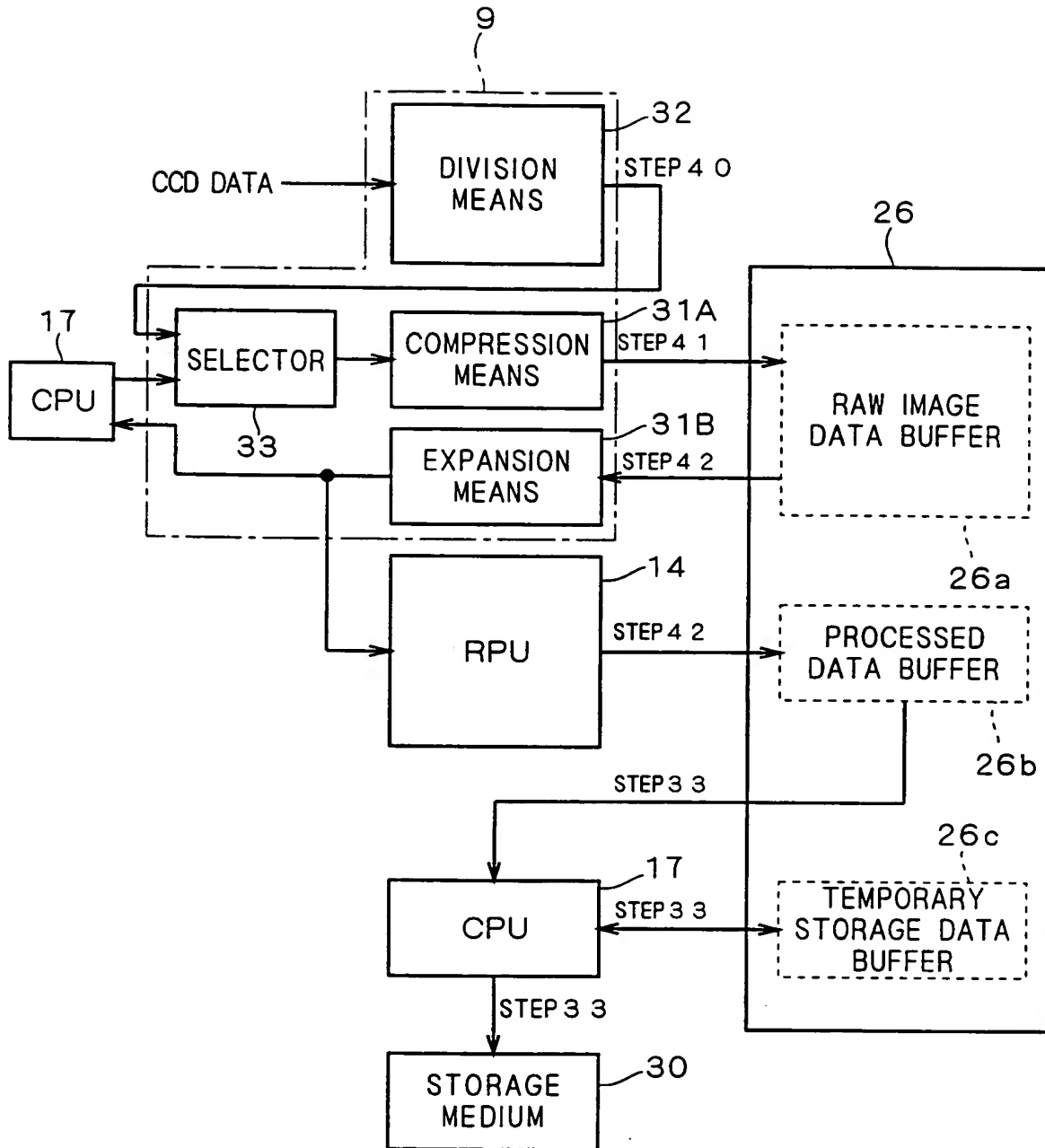
F I G . 5



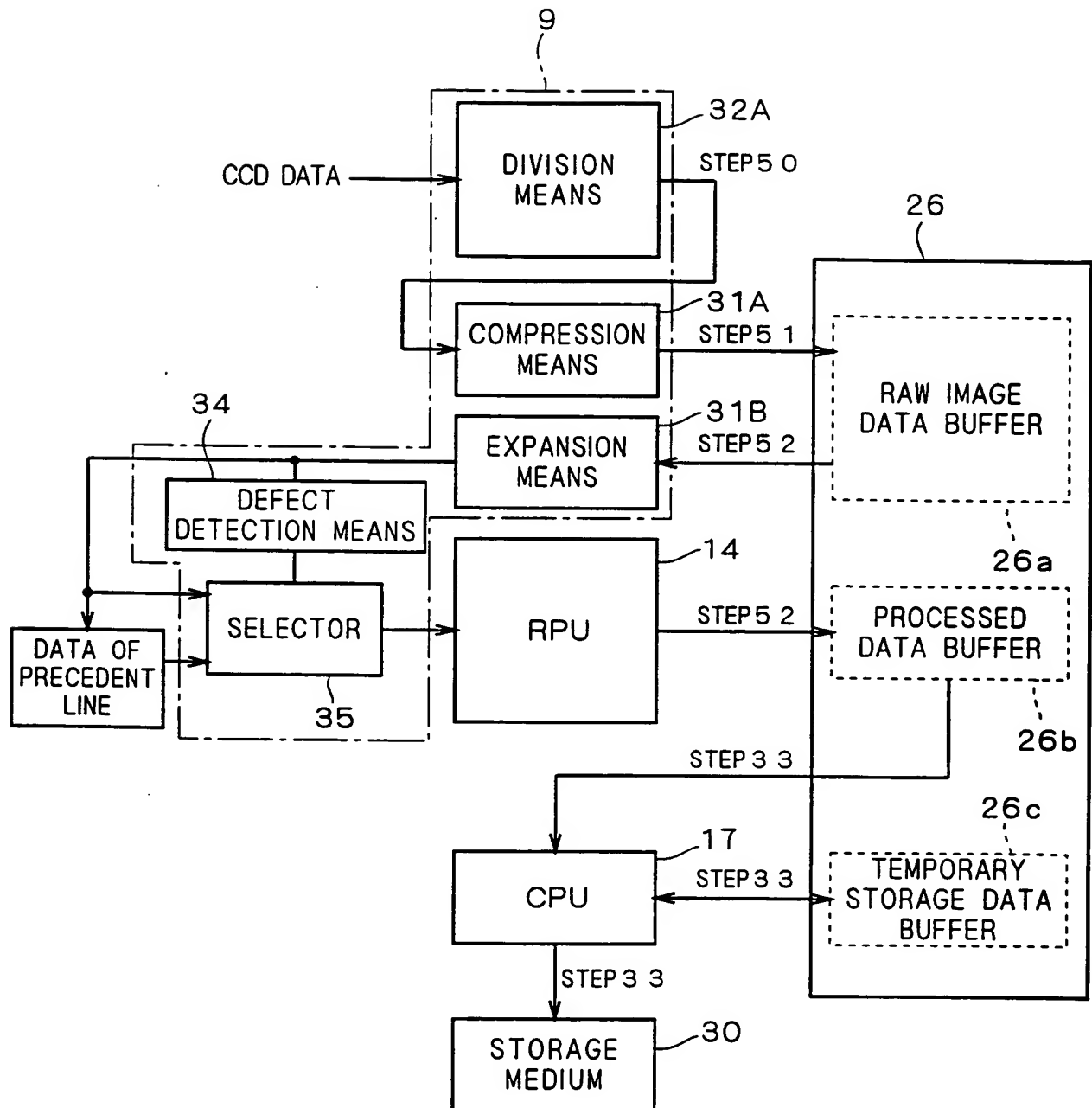
F I G . 6



F I G . 7

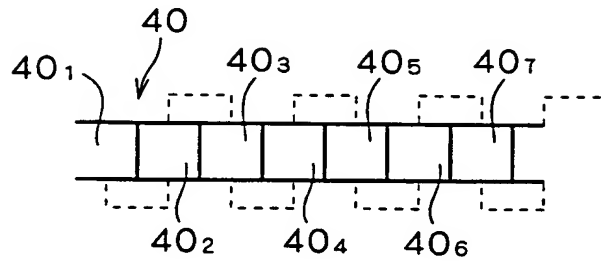


F I G . 8

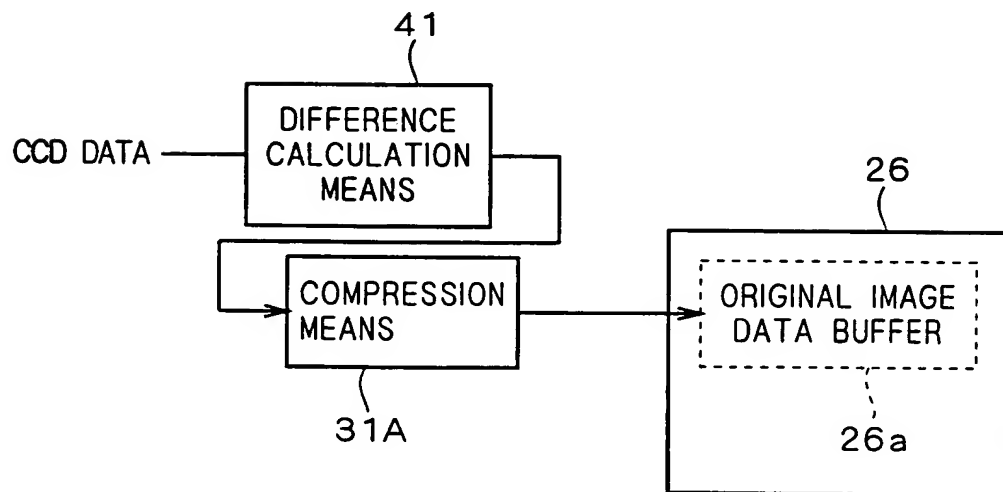


F I G . 9 A

CALCULATE DIFFERENCE BETWEEN ADJACENT PIXELS

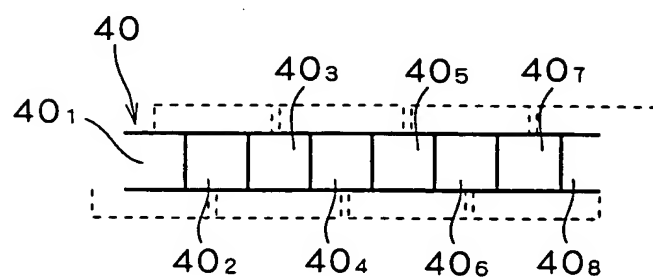


F I G . 9 B

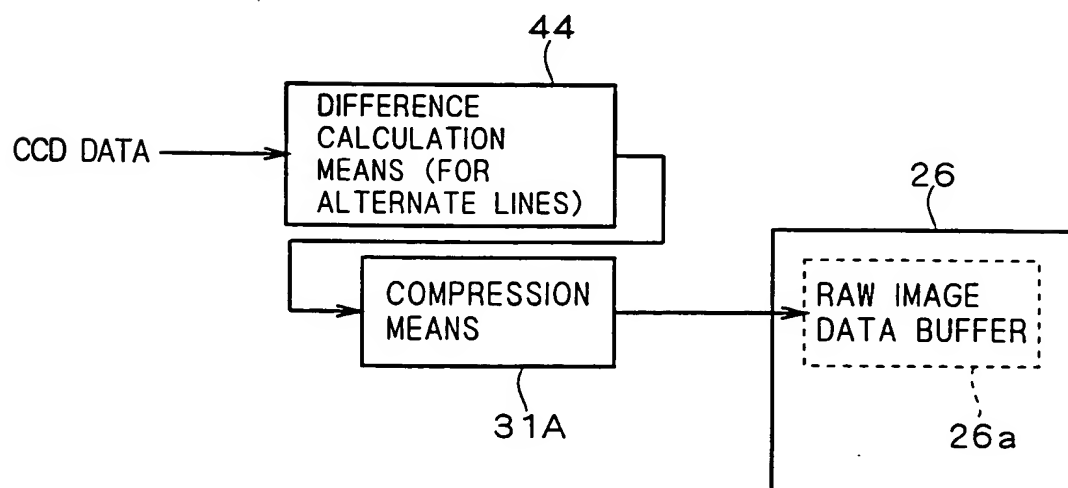


F I G . 1 0 A

CALCULATE DIFFERENCE BETWEEN ALTERNATE PIXELS

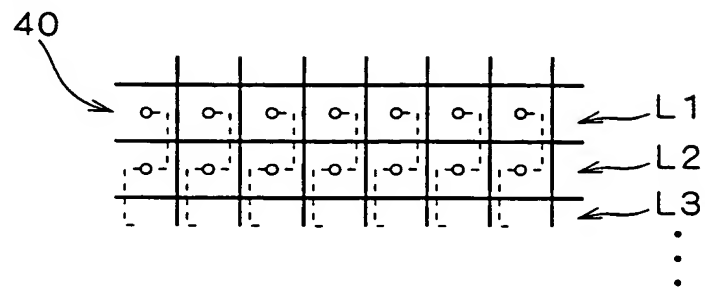


F I G . 1 0 B

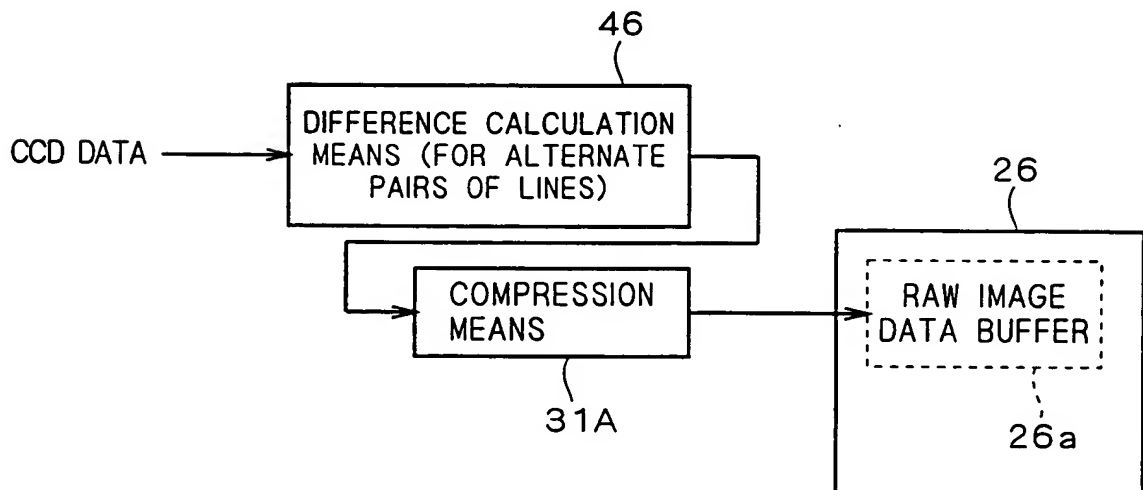


F I G . 1 1 A

CALCULATE DIFFERENCE BETWEEN VERTICAL PAIRS OF PIXELS
ON ADJACENT PAIRS OF LINES

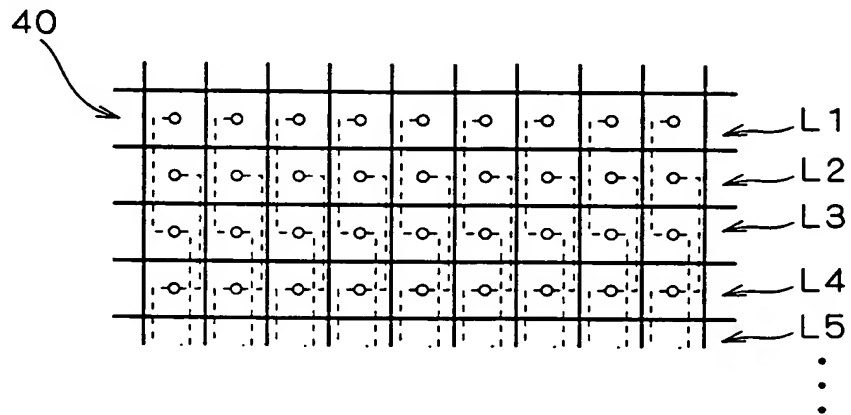


F I G . 1 1 B

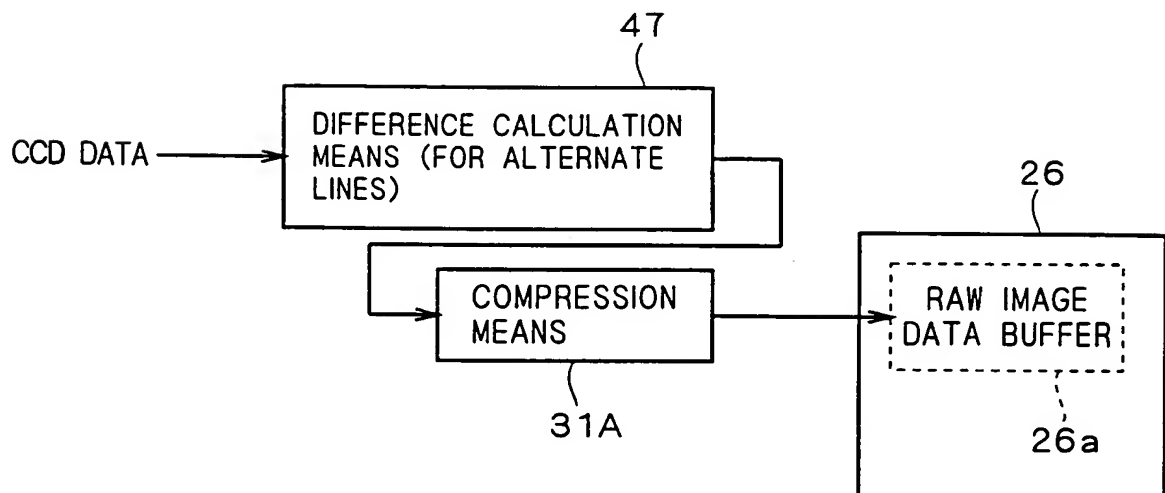


F I G . 1 2 A

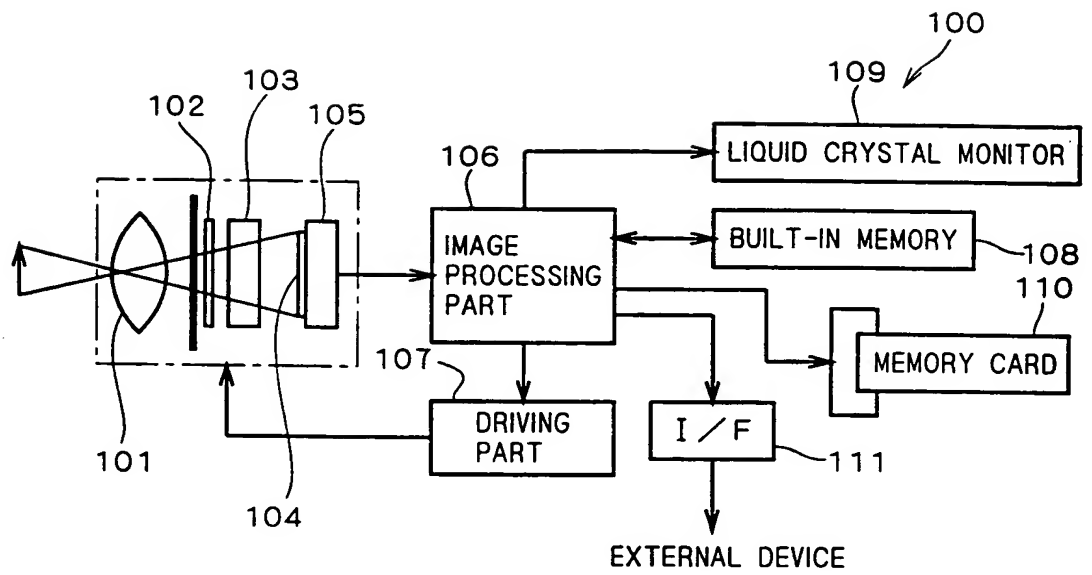
CALCULATE DIFFERENCE BETWEEN VERTICAL PAIRS OF PIXELS
ON ALTERNATE PAIRS OF LINES



F I G . 1 2 B



F I G . 1 3



F I G . 1 4

